

DAY 1

The first day of the workshop dealt with “ The Theory Of Everything”. 4 major topics were discussed.

1. Physics

The principle of the Self Balancing Bot, i.e. Inverted Pendulum. The Vertical position is the position of Unstable equilibrium. We intend to use accelerometer and gyroscope to interface and measure the angle made by the bot with the vertical. Gyroscope to be used as it gives a precise reading while accelerometer gives an accurate but less precise reading. So a complementary filter has to be used to get the actual value of “theta” at all times.

Complementary Filter :

$$angle = 0.98 * (angle + gyrData * dt) + 0.02 * (accData)$$

2. Bitwise Operators

The discussed Bitwise Operators were “^”, “|”, “&”, “~”, “>>”, “<<”

“^” - Bitwise XOR Operator .

Truth Table :

Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	0

“|” - Bitwise OR Operator

Truth Table:

A	B	X = A+B
0	0	0
0	1	1
1	0	1
1	1	1

“&” - Bitwise AND Operator

Truth Table:

A	B	out
0	0	0
0	1	0
1	0	0
1	1	1

“~” - Bitwise NOT Operator

Truth Table:

Input	Output
0	1
1	0

“<<”, “>>” - Left Shift/Right Shift Operators

Operators which can shift the whole binary thread left or right appending or proceeding it by zeroes by the given parameters.

3. Basic Coding

Constants, Variables, Loops & Condition Statements were discussed.

4. AVR Coding

Basic Etiquettes of AVR coding were discussed. So were common common practices. Then Registers “PORTX”, “DDRX”, “PINX” were discussed.

“DDRX” - Stores the pinMode of each pin in the port ‘X’, 1 for output and 0 for input.

“PORTX” - Write only Register, 1 if output is high else 0, can be set for pins in output mode only.

“PINX” - Read Only Register, 1 if input is high, 0 if low, can be read for pins in input mode only in port “X”.

5. Setting, Clearing, Checking, Toggling a bit

Setting : $a|=(1<<x)$

Clearing: $a\&=\sim(1<<x)$

Checking: $a\&=(1<<x)$

Toggling: $a^{\wedge}=(1<<x)$

If ‘X’ is the position of the bit to be toggled.

Programs for basic I/O functions on ATmega16 (LED)

1. Switching LED On:

```
"
%f ghlpg"HaERW38222222WN"
%0penwf g">cxt lkqj @'
%0penwf g">wknlf grc { j @'
%f ghlpg"ugvk'02"
kp'vo clp*xqkf +'
}"
"      FFTD?ugvk=#
      RQTVd?ugvk=#
      y j kg*3+"
"      }"
"      IIVQF Q<<Rrgcug'y tkg"{qwt'Cr r necvkqp"eqf g"
      i"
i"
```

2. Blinking LED's

```
"
%f ghlpg"HaERW38222222WN"
%0penwf g">cxt lkqj @'
%0penwf g">wknlf grc { j @'
%f ghlpg"ugvk'02"
kp'vo clp*xqkf +'
}"
"      FFTD?ugvk=#
      RQTVd?ugvk=#
      y j kg*3+"
"      }"
"      "IIVQF Q<<Rrgcug'y tkg"{qwt'Cr r necvkqp"eqf g"
      af grc { ao u*722=#
      RQTVd? *0RQTVd=#
      i"
i"
```

3. Pattern LED's

%f ghpg"HaERW3822222WN"

%pewf g">cxt lkqj @'

%pewf g">wnlf grc {j @'

%f ghpg'ugvk'c2"

%f ghpg'ugvk3'2"

kp'vo clp*xqkf +'

}"

FFTD?ugvk="

RQTVd?ugvk3="

hqt'kp'vk?2=k>: =k - +'

}"

hqt'kp'v1?k=l>: =l - - +'

}"

RQTVd? *3>>l="

af grc {ao u*422="

RQTVd` ? *3>>l="

"

i "

hqt'kp'v'm?9=m@k=m/+'

}"

RQTVd? *3>>m="

af grc {ao u*422="

RQTVd` ? *3>>m="

i "

RQTVd? *3>>k="

af grc {ao u*422="

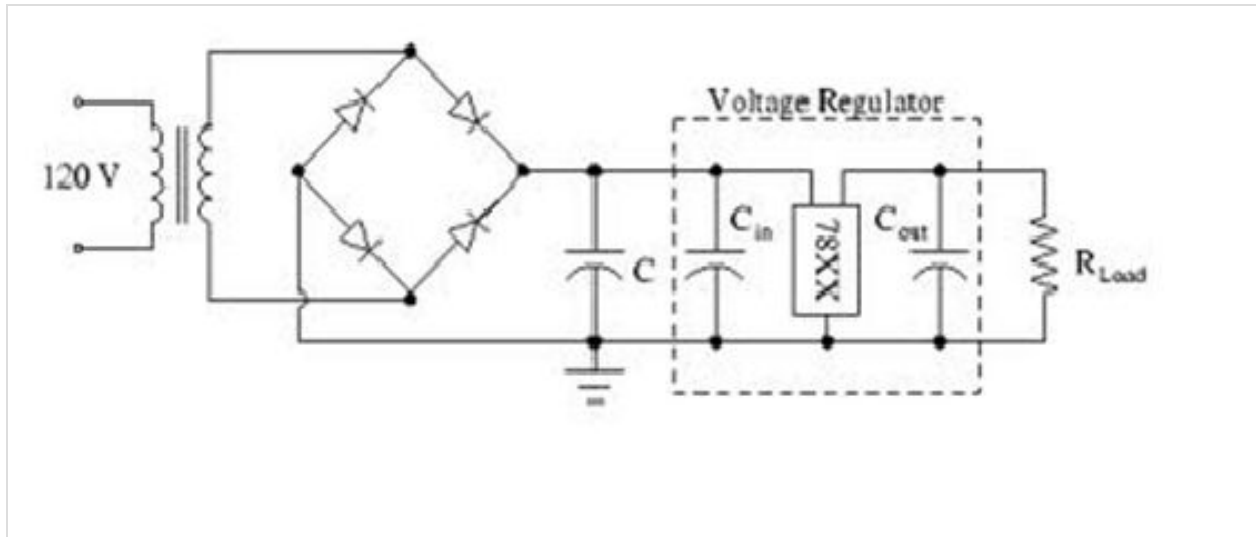
i "

i "

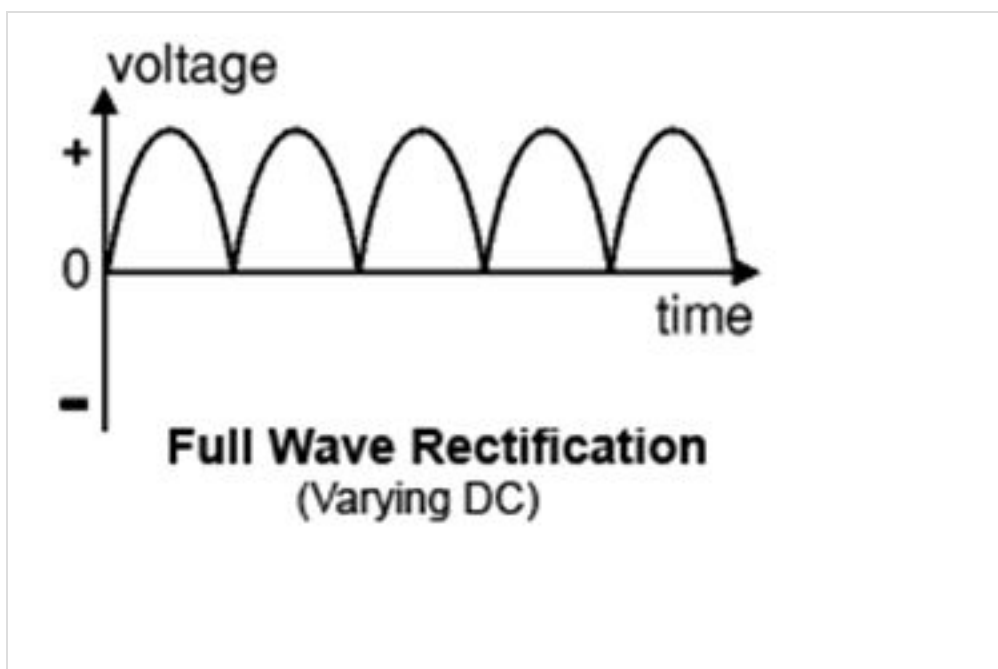
DAY 2

Rectifier Circuit :

They convert A.C. voltage into regulated D.C voltage. A rectifier uses the polar property of a diode i.e. a diode allows only unidirectional current to pass through it which happens when the P- terminal is at higher voltage than the N- terminal of the diode. This configuration is known as forward bias of the diode. The following shows a basic circuit for the rectifier circuit.



The diodes at the right top and left bottom are in forward bias in the positive half cycle and the diodes at the left top and the bottom right are in forward bias in the negative half cycle of the voltage. Hence current always flows in one direction in the circuit. The first capacitor is known as filter which converts the varying signals (as shown below) to ripple voltage.



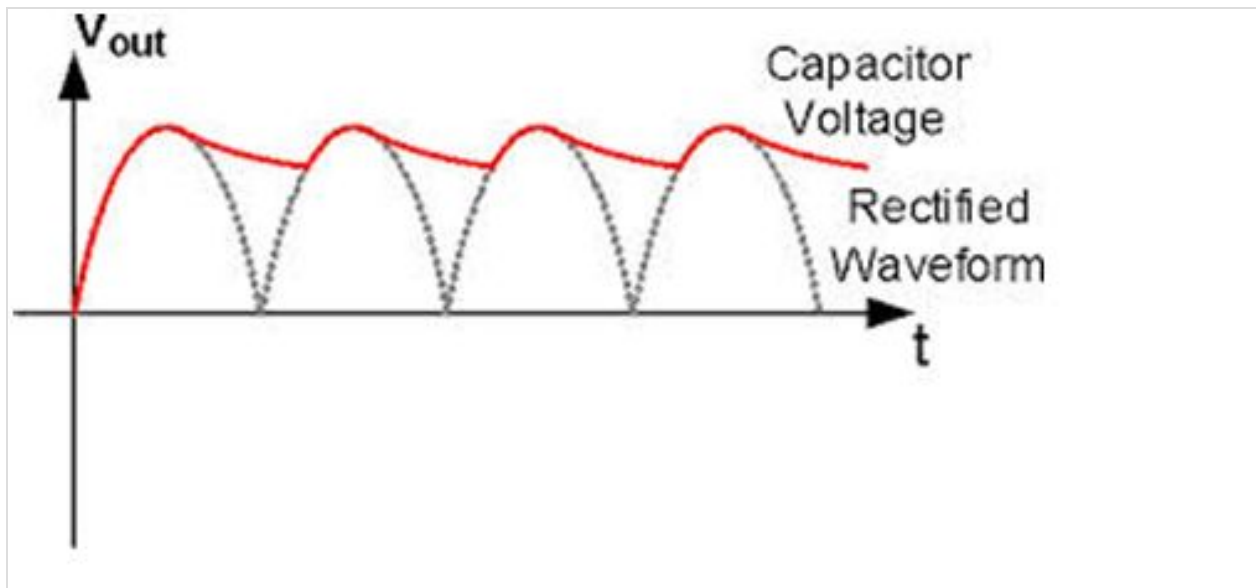
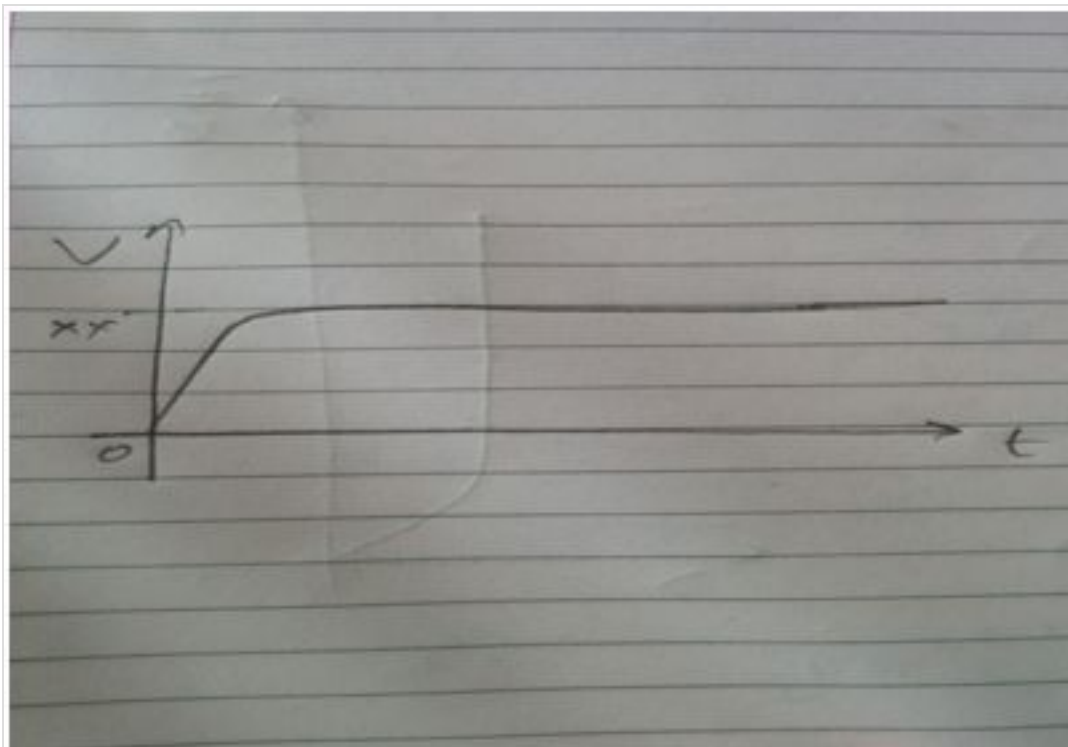


Fig 1 shows voltage after only rectifier and fig 2 shows voltage after filtering the voltage using a capacitor. The filtering works on the property of capacitor to store charge when voltage across terminals is increasing and give it away when the reverse happens i.e. the voltage across its terminals decreases.

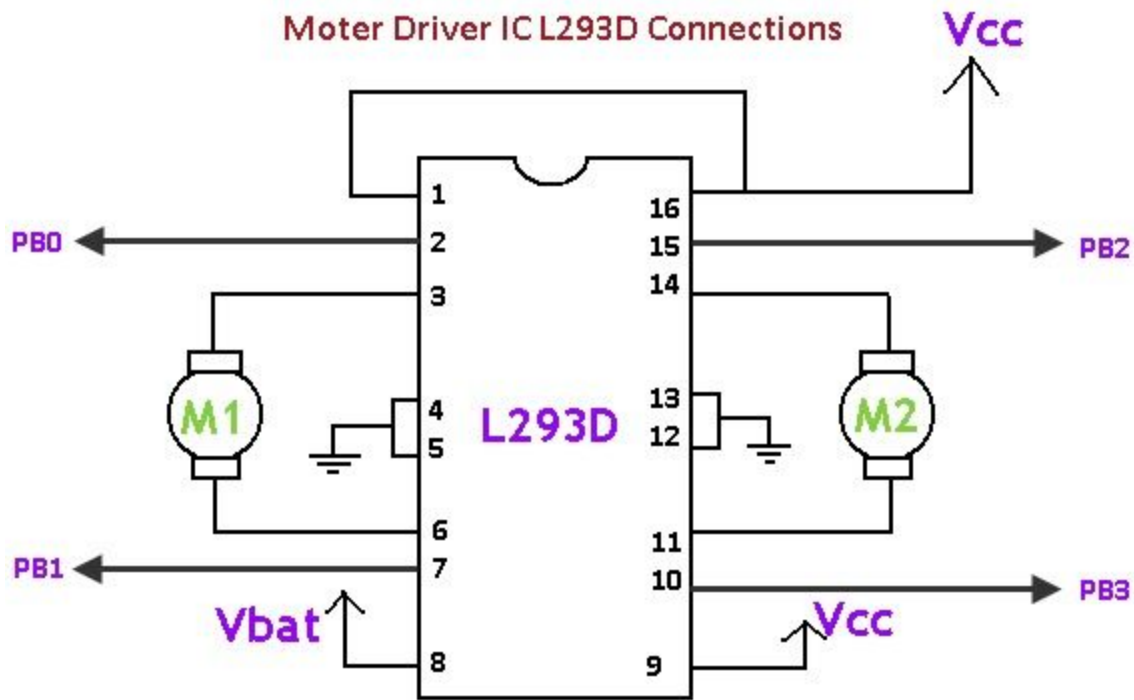
This is followed by a 78xx I.C. which is voltage regulator, where xx denotes its output voltage. It removes the ripples from the voltage and the voltage looks like:



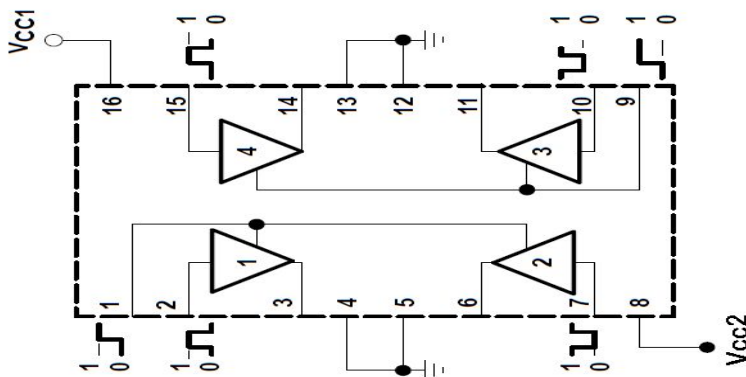
Hence we arrive at a regulated voltage as we wished to. The capacitor after this I.C. is used to take away whatever little ripples are left.

Motor Driver IC's (L293D) :

The motor Driver Circuit L293D is a quad comparator IC which is used to drive motors forward and backward as required. Internally it contains 4 H bridges which are used to drive motors. Block Diagram is shown Below :



The job of the Comparator is to compare the input voltage with a reference voltage and give a logical high if the Input voltage is greater than the reference voltage and a logical low otherwise. The comparator H bridge is shown below.



The Two motors as shown in the above figure are connected to the output pins and the direction of the motor is decided by the voltage that is supplied to the pins I1, I2, I3, I4.

I1, I2 - For motor 1

I3, I4 - For motor 2.

This motor driver IC can be interfaced with out ATmega16 Development Board and a code can be written as follows to run the motors as required.

Note : A PWM across the motors can be generated using Enable pins on this IC.

Code :

```
%f ghpg"HaERW3822222WN"
%openwf g">cxt lkj @'
%openwf g">wnlf grc { j @'
%f ghpg"ugvk"2"
%f ghpg"ugvk3"2"
xqkf "Y *+"
}"
    RQTV E? *3>>RE2+*3>>RE6+="#
"
i "
xqkf "C*+"
}"
    RQTV E? *3>>RE2+*3>>RE7+="#
"
i "
xqkf "U*+"
}"
    RQTV E? *3>>RE3+*3>>RE7+="#
i "
xqkf "F *+"
}"
    RQTV E? *3>>RE3+*3>>RE6+="#
i "
kp'vo clp*xqkf +"
}"
    FFTE?ugvk=#
    FFTF?ugvk=#
    RQTV E?ugvk3=#
    RQTV F? *3>>RF6+*3>>RF7+="#
""y j kg*3+"
""} "
"
    "Y *+"
    af grc { ao u*722+="#
    C*+"
```



```

af gr{ ao u*722+=""
U*=""
af gr{ ao u*722+=""
F *=""
af gr{ ao u*722+=""
IVQF Q<<Rrgcug'y tkg" { qwt"cr r rlec vqp"eqf g""

```

```

"" "
i "

```

ADC (Analog To Digital Conversion) :

The ATmega16 has the capability to take analog input from some of its pins and some of the pins have been reserved for this purpose. These pins are PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA 7.

These pins can take analog inputs and convert it into a 10 bit digital output i.e. a potential difference of 0 - 5 V can be converted into a data packet which has readings from 0 to 1023.

Specific Registers are set in the ATmega16 chip which carry out this conversion and store the result . These registers are explained below.

ADMUX – ADC Multiplexer Selection Register

The ADMUX register is as follows.

Bit	7	6	5	4	3	2	1	0	
	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	ADMUX
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

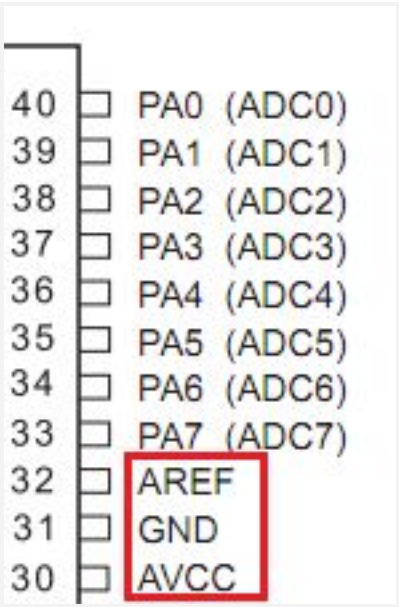
ADMUX Register

The bits that are highlighted are of interest to us. In any case, we will discuss all the bits one by one.

- **6 Jlg' +. * ' E' F9: G%\$ ' E' FYZfYbW' GY'W]cb' 6 Jlg** – These bits are used to choose the reference voltage. The following combinations are used.

REFS1	REFS0	Voltage Reference Selection
0	0	AREF, Internal Vref turned off
0	1	AVCC with external capacitor at AREF pin
1	0	Reserved
1	1	Internal 2.56V Voltage Reference with external capacitor at AREF pin

Reference Voltage Selection



ADC Voltage Reference Pins

The ADC needs a reference voltage to work upon. For this we have a three pins AREF, AVCC and GND. We can supply our own reference voltage across AREF and GND. For this, we can connect a capacitor across AREF pin and ground it to prevent from noise, or you may choose to leave it unconnected. If you want to use the VCC (+5V), we can connect a capacitor across AREF and AVCC. Or else, we can use the internal Vref. Let's choose the second option for Vcc = 5V.

- **6]h) 'È'58 @ F' È'587' @Zi5X1 ghFYgi `h** – Make it '1' to Left Adjust the ADC Result. We will discuss about this a bit later.
- **6]rg' (. \$' È' AI L (. \$' È'5 bUc['7\ UbbY' UbX' ; U]b' GY'W]cb' 6]rg** – There are 8 ADC channels (PA0...PA7). You can choose one specific channel by setting these bits. Since

there are 5 bits, it consists of $2^5 = 32$ different conditions. However, we are concerned only with the first 8 conditions. Initially, all the bits are set to zero.

ADCSRA – ADC Control and Status Register A

The ADCSRA register is as follows.

Bit	7	6	5	4	3	2	1	0	
	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	ADCSRA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

ADCSRA Register

The bits that are highlighted are of interest to us. In any case, we will discuss all the bits one by one.

- Bit 7 (ADEN)** – As the name says, it enables the ADC feature. Unless this is enabled, ADC operations cannot take place across PORTA i.e. PORTA will behave as GPIO pins.
- Bit 6 (ADSC)** – Write this to '1' before starting any conversion. This 1 is written as long as the conversion is in progress, after which it returns to zero. Normally it takes 13 ADC clock pulses for this operation. But when you call it for the first time, it takes 25 as it performs the initialization together with it.
- Bit 5 (ADATE)** – Setting it to '1' enables auto-triggering of ADC. ADC is triggered automatically at every rising edge of clock pulse. View the SFIOR register for more details.
- Bit 4 (ADIF)** – Whenever a conversion is finished and the registers are updated, this bit is set to '1' automatically. Thus, this is used to check whether the conversion is complete or not.
- Bit 3 (ADIE)** – When this bit is set to '1', the ADC interrupt is enabled. This is used in the case of interrupt-driven ADC.
- Bits 2-0 (ADPS2, ADPS1, ADPS0)** – The prescaler (division factor between XTAL frequency and the ADC clock frequency) is determined by selecting the proper combination from the following.

ADPS2	ADPS1	ADPS0	Division Factor
0	0	0	2
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

ADC Prescaler Selections

Assuming XTAL frequency of 16MHz and the frequency range of 50kHz-200kHz, we choose a prescaler of 128.

Thus, $F_{ADC} = 16M/128 = 125kHz$.

And the Last but very Important register THE ADC Register;

ADCL and ADCH – ADC Data Registers

The result of the ADC conversion is stored here. Since the ADC has a resolution of 10 bits, it requires 10 bits to store the result. Hence one single 8 bit register is not sufficient. We need two registers – ADCL and ADCH (ADC Low byte and ADC High byte) as follows. The two can be called together as ADC.

Bit	15	14	13	12	11	10	9	8	
	-	-	-	-	-	-	ADC9	ADC8	ADCH
	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	ADCL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R	R	
	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

ADLAR = 0

ADC Data Registers (ADLAR = 0)

Bit	15	14	13	12	11	10	9	8	
	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADCH
	ADC1	ADC0	-	-	-	-	-	-	ADCL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R	R	
	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	<i>ADLAR = 1</i>

ADC Data Registers (ADLAR = 1)

You can very well see the the effect of ADLAR bit (in ADMUX register). Upon setting ADLAR = 1, the conversion result is left adjusted.

Note : AS SOON AS THE ADCH REGISTER IS READ BY THE MICROCONTROLLER THE VALUES OF ADCH AND ADCL ARE DUMPED. Hence while using ADLAR =1 mode we can get an accuracy of 2^8 only.

A sample Code That Uses ADC is given Below.

```

%f ghlpg'HaERW3822222WN"
%kpenwf g">wknlf grc{g @'
%kpenwf g">ext lkqg @'
%f ghlpg'ugvk'c2"
%f ghlpg'ugvk3"2"
kp'vo ckp*xqkf +"
}"
    FFTD"? "ugvk="
    FFTC"? "ugvk3="
    RQTVd"? "ugvk3="
    CF EUTC"? *3>>CF GP +*3>>CF RU2+*3>>CF RU3+*3>>CF RU4+="
    CF O WZ"? *3>>TGHU2+="
    y j kg*3+"
}"
    IIVQF Q<<Rngcug'y tkg"{qwt'cr r nkcvkqp"eqf g"
    CF EUTC"? *3>>CF UE+="
    kp'c"? "CF E="
    kh'*c@ 42+"
}"
    RQTVd? *3>>RD2+*3>>RD3+*3>>RD4+*3>>RD5+*3>>RD6+="
    i "
    gmg'kh'*c@37+"

```

```

}
    RQTV D? *3>>RD2+*3>>RD3+*3>>RD4+*3>>RD5+!
i
gng'kh'*c@632+
}
    RQTV D? *3>>RD2+*3>>RD3+*3>>RD4+!
i
gng'kh'*c@427+
}
    RQTV D? *3>>RD2+*3>>RD2+!
i
gng"
}
    RQTV D? *3>>RD2+!
i
i
i

```

This code utilises the data given by the POTENTIOMETER AT PA0 and lights up status LED's.

Timer0/ 8 - Bit Timer with PWM.

- Timers are made up of registers, whose value automatically increases/decreases. Thus, the terms timer/counter are used interchangeably.
- In AVR, there are three types of timers – TIMER0, TIMER1 and TIMER2. Of these, TIMER1 is a 16-bit timer whereas others are 8-bit timers.
- Prescalers are used to trade duration with resolution.
- As we want less precision but higher values we choose our prescalers to be high in the range of 256 to 1024.

TCNT0 Register

The **TCNT0** Register – TCNT0 is as follows:

Bit	7	6	5	4	3	2	1	0	
	TCNT0[7:0]								TCNT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

TCNT0 Register

This is where the 8-bit counter of the timer resides. The value of the counter is stored here and increases/decreases automatically. Data can be both read/written from this register.

TCCR0 Register

The TCCR0 Register – TCCR0 is as follows:

Bit	7	6	5	4	3	2	1	0	
	FOC0 WGM00 COM01 COM00 WGM01 CS02 CS01 CS00								TCCR0
Read/Write	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

TCCR0 Register

Right now, we will concentrate on the highlighted bits. The other bits will be discussed as and when necessary. By selecting these three bits, we set the timer up by choosing proper prescaler. The possible combinations are shown below.

CS02	CS01	CS00	Description
0	0	0	No clock source (Timer/Counter stopped).
0	0	1	clk _{I/O} /(No prescaling)
0	1	0	clk _{I/O} /8 (From prescaler)
0	1	1	clk _{I/O} /64 (From prescaler)
1	0	0	clk _{I/O} /256 (From prescaler)
1	0	1	clk _{I/O} /1024 (From prescaler)
1	1	0	External clock source on T0 pin. Clock on falling edge.
1	1	1	External clock source on T0 pin. Clock on rising edge.

Clock Select Bit Description

These bits can be set to either “00” or “01” depending upon the type of PWM you want to generate. Here’s the look up table.

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Truth Table:

A	B	X = A+B
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1	0	1
1	1	1

“&” - Bitwise AND Operator

Truth Table:

A	B	out
0	0	0
0	1	0
1	0	0
1	1	1

“~” - Bitwise NOT Operator

Truth Table:

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0	1
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%penwf g">wnlf grc {j @'
%f ghpg"ugvk'c2"
kp'vo clp*xqkf +'
}"
"    FFTD?ugvk="
"    RQTVd?ugvk="
"    y j kg*3+"
"    }"
"    IIVQF Q<<Rrgcug'y tkg"{qwt'Cr r necvkqp"eqf g"
"    i"
i"
```

2. Blinking LED's

```
"
%f ghpg"HaERW3822222WN"
%penwf g">cxt lkqj @'
%penwf g">wnlf grc {j @'
%f ghpg"ugvk'c2"
kp'vo clp*xqkf +'
}"
"    FFTD?ugvk="
"    RQTVd?ugvk="
"    y j kg*3+"
"    }"
"    IIVQF Q<<Rrgcug'y tkg"{qwt'Cr r necvkqp"eqf g"
"    af grc {ao u*722="
"    RQTVd? *cRQTVd="
"    i"
i"
```

3. Pattern LED's

```
%f ghpg"HaERW3822222WN"
```

%penwf g">ext lkq @'
%penwf g">wnlf grc { @'
%f ghkg"ugvk'c2"
%f ghkg"ugvk3"2"
kpvo clp*xqkf +"
}"

FFTD?ugkv=" "
RQTVd?ugvk3=" "
hqt"*kpvk'2=k>: =k - +"
}"

hqt"*kpv1?k=l>: =l- - +"
}"

RQTVd? *3>>l=" "
af grc { ao u*422=" "
RQTVd` ? *3>>l=" "

i "
hqt"*kpv'm'9="m@k="m/+"
}"

RQTVd? *3>>m=" "
af grc { ao u*422=" "
RQTVd` ? *3>>m=" "

i "
RQTVd? *3>>k=" "
af grc { ao u*422=" "

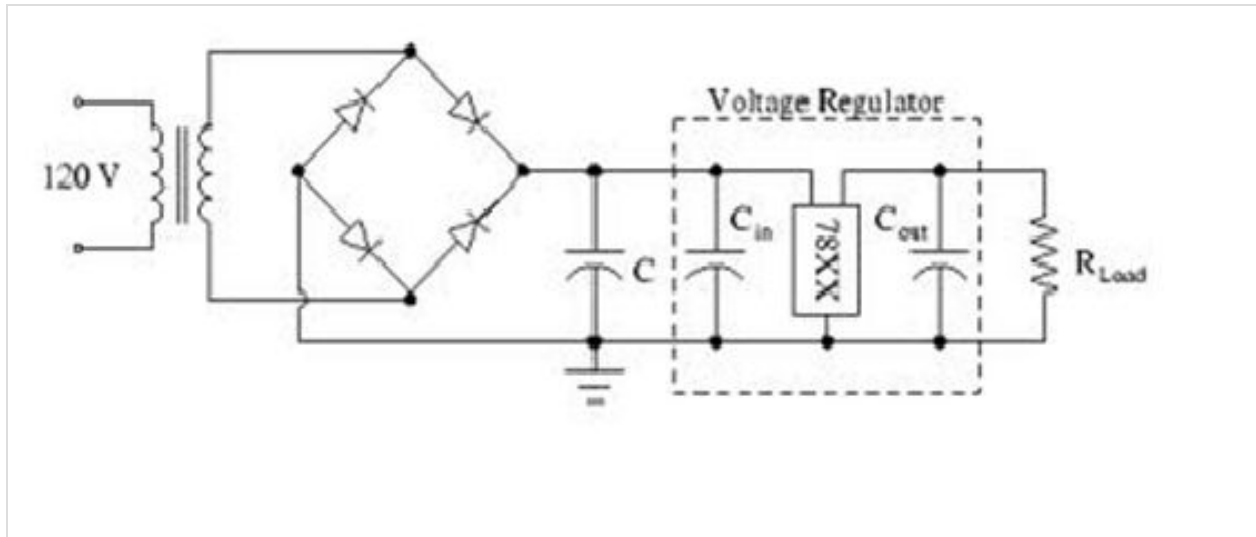
i "

i "

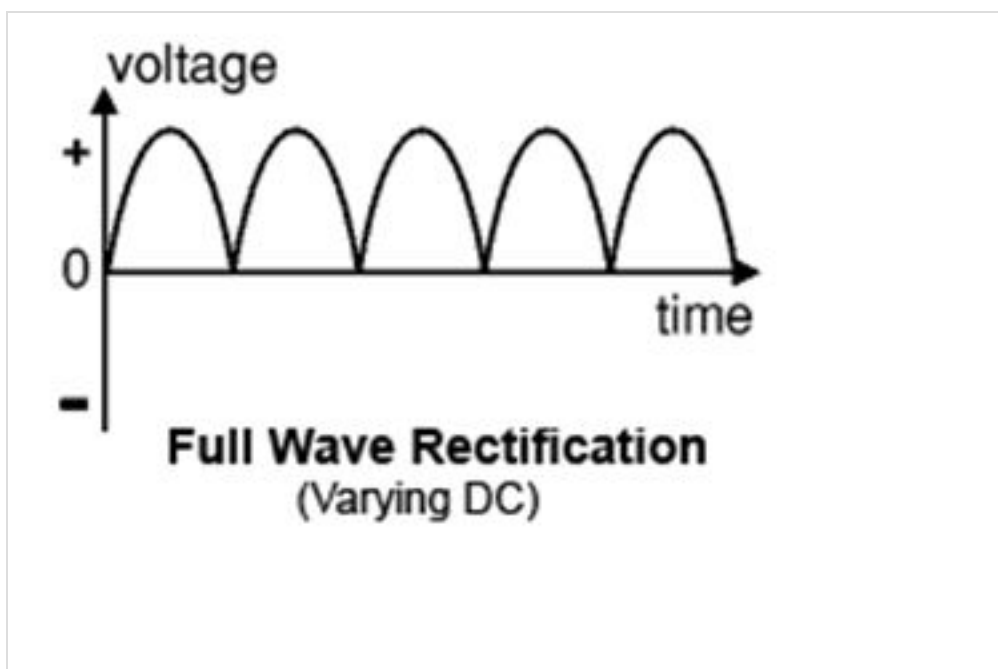
DAY 2 & 3

Rectifier Circuit :

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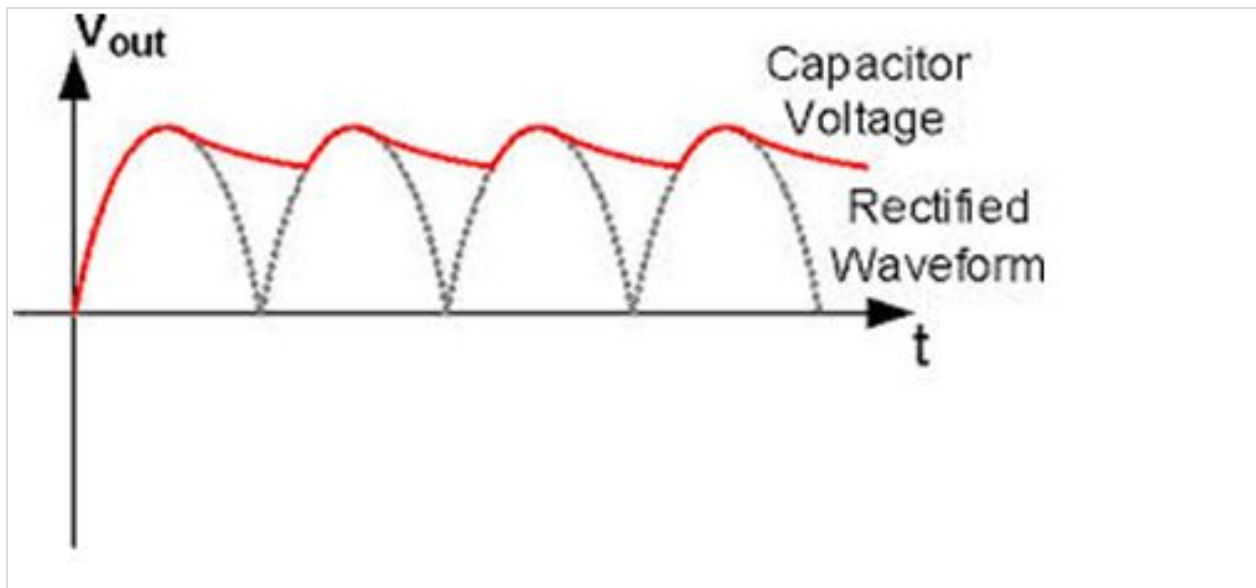
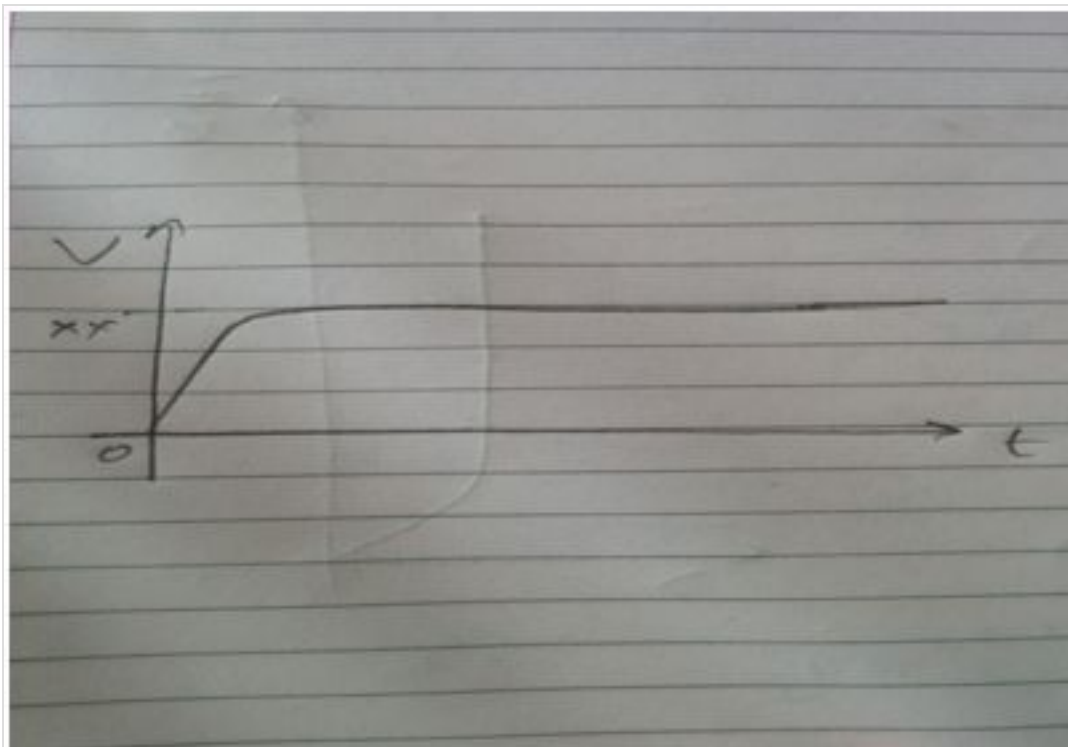


Fig 1 shows voltage after only rectifier and fig 2 shows voltage after filtering the voltage using a capacitor. The filtering works on the property of capacitor to store charge when voltage across terminals is increasing and give it away when the reverse happens i.e. the voltage across its terminals decreases.

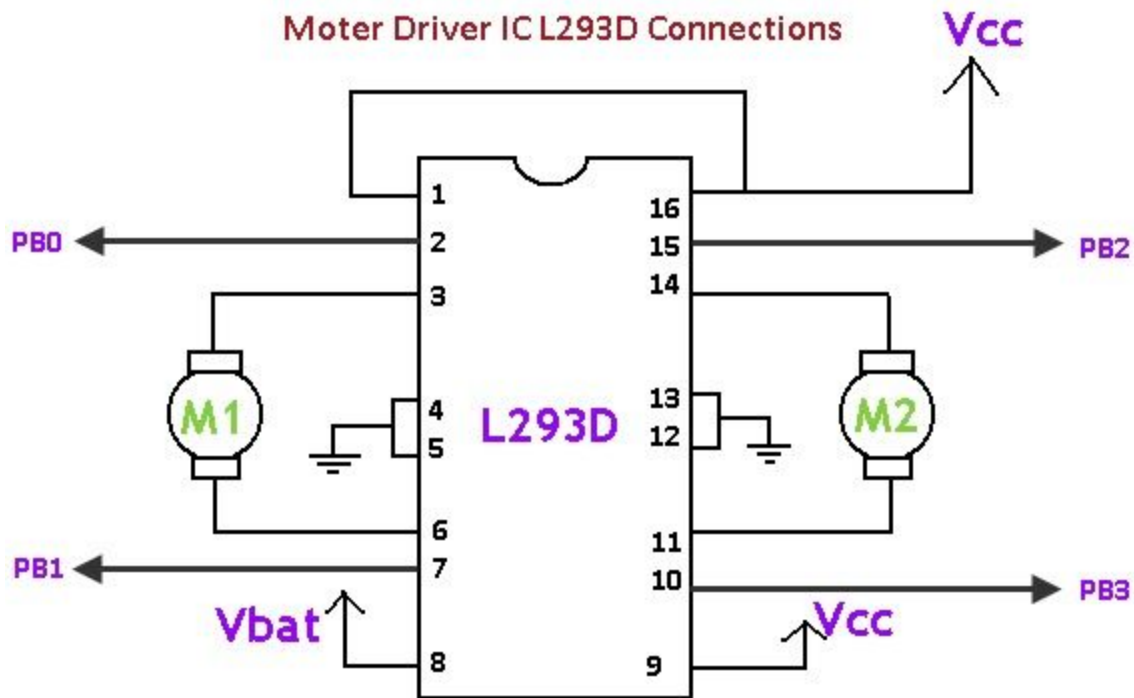
This is followed by a 78xx I.C. which is voltage regulator, where xx denotes its output voltage. It removes the ripples from the voltage and the voltage looks like:



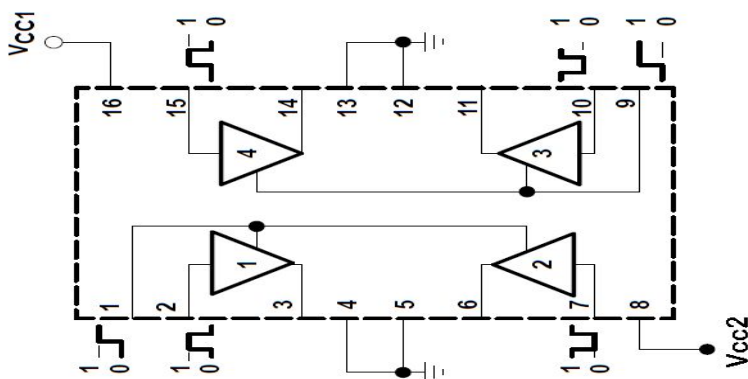
Hence we arrive at a regulated voltage as we wished to. The capacitor after this I.C. is used to take away whatever little ripples are left.

Motor Driver IC's (L293D) :

The motor Driver Circuit L293D is a quad comparator IC which is used to drive motors forward and backward as required. Internally it contains 4 H bridges which are used to drive motors. Block Diagram is shown Below :



The job of the Comparator is to compare the input voltage with a reference voltage and give a logical high if the Input voltage is greater than the reference voltage and a logical low otherwise. The comparator H bridge is shown below.



The Two motors as shown in the above figure are connected to the output pins and the direction of the motor is decided by the voltage that is supplied to the pins I1, I2, I3, I4.

I1, I2 - For motor 1

I3, I4 - For motor 2.

This motor driver IC can be interfaced with out ATmega16 Development Board and a code can be written as follows to run the motors as required.

Note : A PWM across the motors can be generated using Enable pins on this IC.

Code :

```
%f ghpg"HaERW3822222WN"
%openwf g">cxt lkj @'
%openwf g">wnlf grc {j @'
%f ghpg"ugvk"2"
%f ghpg"ugvk3"2"
xqkf "Y *+"
}"
    RQTV E? *3>>RE2+*3>>RE6+="#
"
i "
xqkf "C*+"
}"
    RQTV E? *3>>RE2+*3>>RE7+="#
"
i "
xqkf "U*+"
}"
    RQTV E? *3>>RE3+*3>>RE7+="#
i "
xqkf "F *+"
}"
    RQTV E? *3>>RE3+*3>>RE6+="#
i "
kp'vo ckp*xqkf +"
}"
    FFTE?ugvk=#
    FFTF?ugvk=#
    RQTV E?ugvk3=#
    RQTV F? *3>>RF6+*3>>RF7+="#
""y j kg*3+"
""} "
"
    "Y *+"
    af grc {ao u*722+="#
    C*+"
```

```

af gr{ ao u*722+=""
U*=""
af gr{ ao u*722+=""
F *=""
af gr{ ao u*722+=""
IVQF Q<<Rrgcug'y tkg" { qwt"cr r rlec vqp"eqf g""

```

```

"" "
i "

```

ADC (Analog To Digital Conversion) :

The ATmega16 has the capability to take analog input from some of its pins and some of the pins have been reserved for this purpose. These pins are PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA 7.

These pins can take analog inputs and convert it into a 10 bit digital output i.e. a potential difference of 0 - 5 V can be converted into a data packet which has readings from 0 to 1023.

Specific Registers are set in the ATmega16 chip which carry out this conversion and store the result . These registers are explained below.

ADMUX – ADC Multiplexer Selection Register

The ADMUX register is as follows.

Bit	7	6	5	4	3	2	1	0	
	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	ADMUX
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

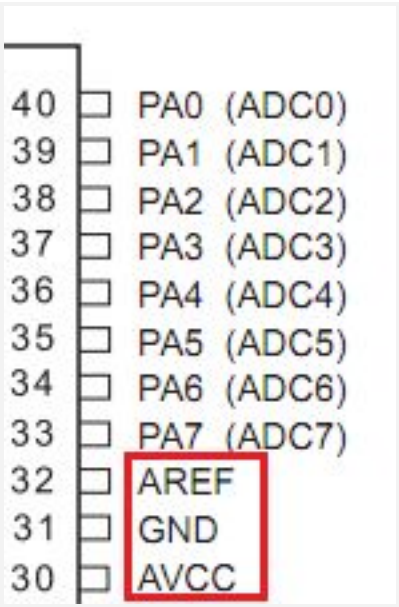
ADMUX Register

The bits that are highlighted are of interest to us. In any case, we will discuss all the bits one by one.

- **6 Jlg' +. * ' E' F9: G%\$ ' E' FYZfYbW' GY'W]cb' 6 Jlg** – These bits are used to choose the reference voltage. The following combinations are used.

REFS1	REFS0	Voltage Reference Selection
0	0	AREF, Internal Vref turned off
0	1	AVCC with external capacitor at AREF pin
1	0	Reserved
1	1	Internal 2.56V Voltage Reference with external capacitor at AREF pin

Reference Voltage Selection



ADC Voltage Reference Pins

The ADC needs a reference voltage to work upon. For this we have a three pins AREF, AVCC and GND. We can supply our own reference voltage across AREF and GND. For this, we can connect a capacitor across AREF pin and ground it to prevent from noise, or you may choose to leave it unconnected. If you want to use the VCC (+5V), we can connect a capacitor across AREF and AVCC. Or else, we can use internal Vref. Let's choose the second option for Vcc = 5V.

- **6]h) 'E'58 @ F 'E'587 ' @Zi5X1 ghFYgi `h** – Make it '1' to Left Adjust the ADC Result. We will discuss about this a bit later.
- **6]rg' (. \$ 'E' AI L (. \$ 'E'5 bUc['7\ UbbY' UbX' ; U]b' GY'W]cb' 6]rg** – There are 8 ADC channels (PA0...PA7). You can choose one specific channel by setting these bits. Since

there are 5 bits, it consists of $2^5 = 32$ different conditions. However, we are concerned only with the first 8 conditions. Initially, all the bits are set to zero.

ADCSRA – ADC Control and Status Register A

The ADCSRA register is as follows.

Bit	7	6	5	4	3	2	1	0	
	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	ADCSRA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

ADCSRA Register

The bits that are highlighted are of interest to us. In any case, we will discuss all the bits one by one.

- Bit 7 (ADEN)** – As the name says, it enables the ADC feature. Unless this is enabled, ADC operations cannot take place across PORTA i.e. PORTA will behave as GPIO pins.
- Bit 6 (ADSC)** – Write this to '1' before starting any conversion. This 1 is written as long as the conversion is in progress, after which it returns to zero. Normally it takes 13 ADC clock pulses for this operation. But when you call it for the first time, it takes 25 as it performs the initialization together with it.
- Bit 5 (ADATE)** – Setting it to '1' enables auto-triggering of ADC. ADC is triggered automatically at every rising edge of clock pulse. View the SFIOR register for more details.
- Bit 4 (ADIF)** – Whenever a conversion is finished and the registers are updated, this bit is set to '1' automatically. Thus, this is used to check whether the conversion is complete or not.
- Bit 3 (ADIE)** – When this bit is set to '1', the ADC interrupt is enabled. This is used in the case of interrupt-driven ADC.
- Bits 2-0 (ADPS2, ADPS1, ADPS0)** – The prescaler (division factor between XTAL frequency and the ADC clock frequency) is determined by selecting the proper combination from the following.

ADPS2	ADPS1	ADPS0	Division Factor
0	0	0	2
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

ADC Prescaler Selections

Assuming XTAL frequency of 16MHz and the frequency range of 50kHz-200kHz, we choose a prescaler of 128.

Thus, $F_{ADC} = 16M/128 = 125kHz$.

And the Last but very Important register THE ADC Register;

ADCL and ADCH – ADC Data Registers

The result of the ADC conversion is stored here. Since the ADC has a resolution of 10 bits, it requires 10 bits to store the result. Hence one single 8 bit register is not sufficient. We need two registers – ADCL and ADCH (ADC Low byte and ADC High byte) as follows. The two can be called together as ADC.

Bit	15	14	13	12	11	10	9	8	
	-	-	-	-	-	-	ADC9	ADC8	ADCH
	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	ADCL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R	R	
	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

ADLAR = 0

ADC Data Registers (ADLAR = 0)

Bit	15	14	13	12	11	10	9	8	
	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADCH
	ADC1	ADC0	-	-	-	-	-	-	ADCL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R	R	
	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	<i>ADLAR = 1</i>

ADC Data Registers (ADLAR = 1)

You can very well see the the effect of ADLAR bit (in ADMUX register). Upon setting ADLAR = 1, the conversion result is left adjusted.

Note : AS SOON AS THE ADCH REGISTER IS READ BY THE MICROCONTROLLER THE VALUES OF ADCH AND ADCL ARE DUMPED. Hence while using ADLAR =1 mode we can get an accuracy of 2^8 only.

A sample Code That Uses ADC is given Below.

```

%f ghlpg'HaERW3822222WN"
%kpenwf g">wknlf grc{G @'
%kpenwf g">ext lkqG @'
%f ghlpg'ugvk'c2"
%f ghlpg'ugvk3"2"
kp'vo ckp*xqkf +"
}"
    FFTD"? "ugvk="
    FFTC"? "ugvk3="
    RQTV D"? "ugvk3="
    CF EUTC"? *3>>CF GP +*3>>CF RU2+*3>>CF RU3+*3>>CF RU4+="
    CF O WZ"? *3>>TGHU2+="
    y j kg*3+"
}"
    IIVQF Q<<Rngcug'y tkg"{qwt'cr r nkecvkqp"eqf g"
    CF EUTC"? *3>>CF UE+="
    kp'c"? "CF E="
    kh'*c@ 42+"
}"
    RQTV D? *3>>RD2+*3>>RD3+*3>>RD4+*3>>RD5+*3>>RD6+="
    i "
    gmg'kh'*c@37+"

```

```

}
    RQTV D? *3>>RD2+*3>>RD3+*3>>RD4+*3>>RD5+!
i
gng'kh'*c@632+
}
    RQTV D? *3>>RD2+*3>>RD3+*3>>RD4+!
i
gng'kh'*c@427+
}
    RQTV D? *3>>RD2+*3>>RD2+!
i
gng"
}
    RQTV D? *3>>RD2+!
i
i
i

```

This code utilises the data given by the POTENTIOMETER AT PA0 and lights up status LED's.

Timer0/ 8 - Bit Timer with PWM.

- Timers are made up of registers, whose value automatically increases/decreases. Thus, the terms timer/counter are used interchangeably.
- In AVR, there are three types of timers – TIMER0, TIMER1 and TIMER2. Of these, TIMER1 is a 16-bit timer whereas others are 8-bit timers.
- Prescalers are used to trade duration with resolution.
- As we want less precision but higher values we choose our prescalers to be high in the range of 256 to 1024.

TCNT0 Register

The **TCNT0** register – TCNT0 is as follows:

Bit	7	6	5	4	3	2	1	0	
	TCNT0[7:0]								TCNT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

TCNT0 Register

This is where the 8-bit counter of the timer resides. The value of the counter is stored here and increases/decreases automatically. Data can be both read/written from this register.

TCCR0 Register

The TCCR0 Register – TCCR0 is as follows:

Bit	7	6	5	4	3	2	1	0	
	FOC0	WGM00	COM01	COM00	WGM01	CS02	CS01	CS00	TCCR0
Read/Write	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

TCCR0 Register

Right now, we will concentrate on the highlighted bits. The other bits will be discussed as and when necessary. By selecting these three bits, we set the timer up by choosing proper prescaler. The possible combinations are shown below.

CS02	CS01	CS00	Description
0	0	0	No clock source (Timer/Counter stopped).
0	0	1	$clk_{I/O}$ /(No prescaling)
0	1	0	$clk_{I/O}/8$ (From prescaler)
0	1	1	$clk_{I/O}/64$ (From prescaler)
1	0	0	$clk_{I/O}/256$ (From prescaler)
1	0	1	$clk_{I/O}/1024$ (From prescaler)
1	1	0	External clock source on T0 pin. Clock on falling edge.
1	1	1	External clock source on T0 pin. Clock on rising edge.

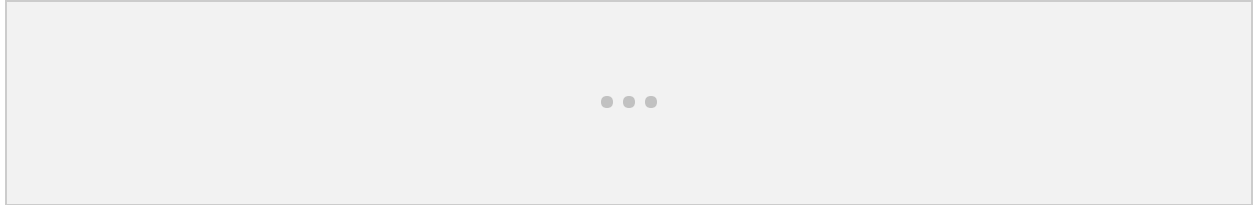
Clock Select Bit Description

Bit 6,3 – WGM01:0 – Waveform Generation Mode – These bits can be set to either “00” or “01” depending upon the type of PWM you want to generate. Here’s the look up table.

Bit 5,4 – COM01:0 – Compare Match Output Mode – These bits are set in order to control the behavior of Output Compare pin in accordance with the WGM01:0 bits.

TIMSK Register

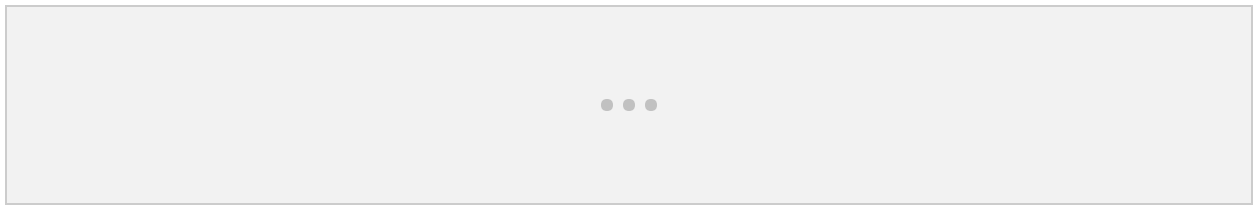
The **TIMSK Register** – TIMSK Register is as follows. It is a common register for all the three timers. For TIMER0, bits 1 and 0 are allotted. Right now, we are interested in the 0th bit **TOIF**. Setting this bit to '1' enables the TIMER0 overflow interrupt.



TIMSK Register

TIFR Register

The **TIFR Register** – TIFR is as follows. Even though we are not using it in our code, you should be aware of it.



TIFR Register

This is also a register shared by all the timers. Even here, bits 1 and 0 are allotted for TIMER0. At present we are interested in the 0th bit **TOIF** bit. This bit is set (one) whenever TIMER0 overflows. This bit is reset (zero) whenever the Interrupt Service Routine (ISR) is executed. If there is no ISR to execute, we can clear it manually by writing one to it

Here Are some sample codes using timers and PWM

1. LED BLINKING WITHOUT DELAY

```
#include <avr/io.h>
#define setit ~0
#define setit1 0
int main(void)
{
    DDRB = setit;
    PORTB= setit1;
```



```
i "
gnug'kh"*c@837+"
}"
VEET2"? "%3>>Y I O 22+*3>>EQO 23+*3>>Y I O 23+*3>>EU22+*3>>EU24+!="
QET2"? "48="
```

```
i "
gnug'kh"*c@632+"
}"
VEET2"? "%3>>Y I O 22+*3>>EQO 23+*3>>Y I O 23+*3>>EU22+*3>>EU24+!="
QET2"? "324="
```

```
i "
gnug'kh"*c@427+"
}"
VEET2"? "%3>>Y I O 22+*3>>EQO 23+*3>>Y I O 23+*3>>EU22+*3>>EU24+!="
QET2"? "375="
```

```
i "
gnug"
}"
VEET2"? "%3>>Y I O 22+*3>>EQO 23+*3>>Y I O 23+*3>>EU22+*3>>EU24+!="
QET2"? "426="
```

```
i "
```

```
i "
```

```
i "
```

3. FADING LED USING PWM

```
%4penwf g>cxt lkqj @
l%4penwf g>cxt lkpgtt wr vj @
%f ghlpg'HaERW3822222WN"
%4penwf g>wnlf grc { j @
%f ghlpg'ugvk'c2"
%f ghlpg'ugvk3"2"
hqcV'F wf{e{erg"? "2="
"
"
kpvo clp*+"
}"
llugk*+="
FFTD"? "ugkv="
VEET2"? "%3>>Y I O 22+*3>>Y I O 23+*3>>EQO 23+*3>>EU22+*3>>EU24+*3>>EQO 22+!="
llVKO UM"? "%3>>VQKG2+!="
QET2"? "%F wf{e{ergB22+, 477="
VEP V2"? "2="
y j kg"*3+"
}"
hqt"%kpvk'2=k>32=k - +"
}"
F wf{e{erg- ?32="
QET2"? "%F wf{e{ergB22+, 477="
```

```

        af gr{ ao u*322+=""
    i ""
    hqt*pv1?2=1>32=1- - +"
    }"
        F w{e{erg/?32=""
        QET2"?*F w{e{ergB22+, 477=""
        af gr{ ao u*322+=""
    i ""
    af gr{ ao u*522+=""
i ""
i ""
i ""

```

agXeehcgf`:

dhffidh are basically events that require immediate attention by the microcontroller. When an interrupt event occurs the microcontroller pause its current task and attend to the interrupt by executing an **dhffidhGYfjJWFcihbYfiGF**. At the end of the ISR the microcontroller returns to the task it had pause and continue its normal operations.

In order for the microcontroller to respond to an interrupt event the interrupt feature of the microcontroller must be enabled along with the specific interrupt. This is done by setting the **ICUdhffidhbUVYX** bit and the **dhffidhbUVY** bit of the specific interrupt.

Qc"i"] oA^i ca^A Uj ~ a^A i A Qc"i"] oP a a^i A

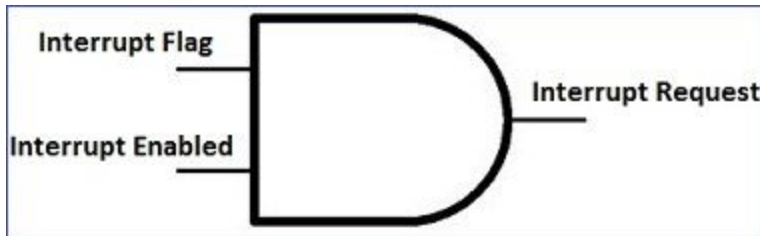
An **dhffidhGYfjJWFcihbYfiGF** or **dhffidh<UbXYf** is a piece of code that should be execute when an interrupt is triggered. Usually each enabled interrupt has its own ISR. In AVR assembly language each ISR **AI GH**end with the **F9H** instruction which indicates the end of the ISR.

Qc"i"] oP a e • A a a A a a^i A a a A

Each interrupt is associated with two (2) bits, an **dhffidh: `Uj `6Jh** and an **dhffidhbUVYX`6Jh**. These bits are located in the I/O registers associated with the specific interrupt:

- The **dhffidhZUj** bit is set whenever the interrupt event occur, whether or not the interrupt is enabled.
- The **dhffidhbUVYX** bit is used to enable or disable a specific interrupt. Basically it tells the microcontroller whether or not it should respond to the interrupt if it is triggered.

In summary basically both the **Interrupt Flag** and the **Interrupt Enabled** are required for an interrupt request to be generated as shown in the figure below.



Ö|| àà/0 c^!!~] d0; aà|^à/0ãÁ

Apart from the enabled bits for the specific interrupts the global interrupt enabled bit **AI GH** be enabled for interrupts to be activated in the microcontroller.

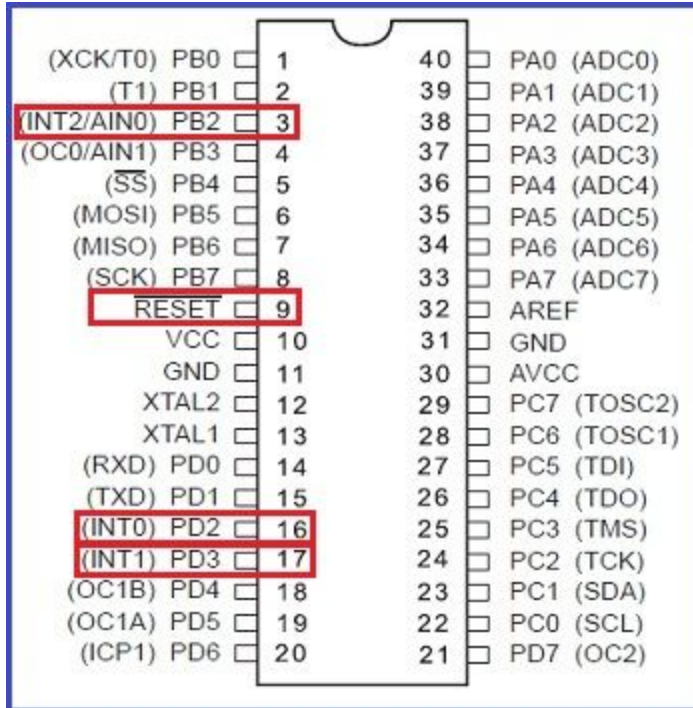
For the AVR 8-bits microcontroller this bit is located in the **Global Interrupt Enabled** is bit 7, the **bit**, in the SREG.



Interrupt sources provided with the AVR microcontroller

The AVR 8-bits microcontroller provide both internal and external interrupt sources. The internal interrupts are associated with the microcontroller's peripherals. That is the **Hja Yf# ci bhYfZ 5 bUc[`7 ca dUfUrcfZ YHW** The external interrupts are triggered via external pins. The figure below shows the pins, on which the external interrupts can be triggered, for an AVR 8-bit microcontroller. On this microcontroller there are four (4) external interrupts:

1. The **F9G9H** interrupt - Triggered from pin 9.
2. **9I hYfbU` bhYffi dh\$ fBH\$L** - Triggered from pin 16.
3. **9I hYfbU` bhYffi dh%fBH%L** - Triggered from pin 17.
4. **9I hYfbU` bhYffi dh&fBH&L** - Triggered from pin 3.



JYfm-a dcfUbh

When writing assembly codes for your AVR microcontroller utilizing the interrupt feature the following **AI GH** be observed:

- The interrupt **AI GH** be enabled by setting its enabled bit in the appropriate I/O register.
- The Global Interrupt bit, the **=bit**, in the microcontroller's status register (SREG) **AI GH** also be enabled.
- The stack **AI GH** be initialized. When an interrupt is being service the microcontroller need to store critical information on the stack and so it must be initialized.
- The Interrupt Service Routine (ISR) **AI GH** end with the **F9H** instruction, which indicates the end of the ISR. The microcontroller needs to know when it reaches the end of the ISR so it can return to its previous task.

Steps taken in servicing an interrupt

Upon the triggering of an interrupt the following sequence is followed by the microcontroller providing that the both the specific interrupt and global interrupts are enabled in the microcontroller:

